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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,510	02/07/2006	Hideo Nagai	92478-9800	8521
53044 7590 03/04/2009 SNELL & WILMER L.L.P. (Panasonic) 600 ANTON BOULEVARD SUITE 1400 COSTA MESA, CA 92626				
EXAMINER HO, HOANG QUAN TRAN				
ART UNIT 2818		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/567,510

Applicant(s)

NAGAI, HIDEO

Examiner

Hoang-Quan T. Ho

Art Unit

2818

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 35-37, 40, 41, 46, 48, 49 and 52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 35-37, 40, 41, 46, 48 and 52 is/are rejected.
- 7) ☒ Claim(s) 49 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

Applicant's amendment to the claims, filed on March 3, 2008, is acknowledged. Entry of amendment is accepted and made of record. Currently, claims 35 – 37, 40 – 41, 46, 48 – 49, and 52 are pending in light of the amendment, in which: claims 35, 41 and 48 – 49 were amended; claims 1 – 34, 38 – 39, 42 – 45, 47, and 50 – 51 were cancelled; no claim was withdrawn; and claim 52 was added.

Response to Arguments/Remarks

Applicant's response filed on December 12, 2008 is acknowledged and is answered as follows.

Applicant's arguments, see pgs. 6 – 14, with respect to the rejections have been fully considered but they are not fully persuasive in view of the following reasons.

Applicant argued that a flexible thin polyimide sheet as a base structure for depositing a multilayer epitaxial semiconductor structure to create a light emitting diode would not be recognized by one of ordinary skill in the art. The examiner respectfully disagrees. Claim 35 is directed to a device recitation, not fabrication. Furthermore, claim 35 does not recite with respect to depositing a multilayer epitaxial semiconductor structure. Assuming *arguendo*, if claim 35 recited limitation drawn to a process by which the product is made (i.e., deposition of a multilayer epitaxial semiconductor structure), even though product by process claims are limited by and defined by the process,

determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Because the product by process does not change the end product, Applicant's claimed invention does not distinguish over prior art. See MPEP § 2113. Claim 35 does not contain limitation(s) that would preclude base structure to be construed as a plastic material as taught by Durocher.

As applicant pointed out, Durocher is directed to post packaging of a pre-existing LED chip. The ability to provide a multilayer epitaxial semiconductor LED chip structure would have been obvious in view of Durocher's disclosure at col. 7, lines 30 – 40 (with the combination of Okazaki's disclosure), on a plastic substrate at col. 7 – 8 under 3. Mounting the LED Chips sub-section. In other words, one of ordinary skill in the art would be capable of choosing a LED chip with the claimed epitaxial semiconductor structure LED (i.e., disclosure of Okazaki) and place it within Durocher's structure (i.e., plastic carrier substrate). This would render applicant's manufacturing arguments perspective virtually moot (i.e., fabrication of the LED chip structure and the carrier packaging are at two different points of time). Therefore, Durocher and Okazaki disclosures meet the claimed limitations of claim 35.

Applicant further argued that their claimed base substrate is more analogous to the Okazaki base substrate shown in Fig. 1. The examiner respectfully disagrees. Claim 35 does not set forth further limitation(s) on a 'base substrate'. However, the examiner

recognizes that claim 49 contains a specified material of a base substrate and the mounting of the multilayer epitaxial structure of claim 48. In light of applicant's arguments with respect to the base substrate material and providing the multilayer epitaxial structure on the base substrate, the rejection of claim 49 has been withdrawn as it has been found persuasive.

Applicant argued with respect to the rejection of claim 51. However, it is irrelevant because applicant cancelled claim 51. Therefore, applicant's arguments with regards to claim 51 has been rendered moot.

In view of the foregoing reasons, the Examiner believes that all Applicant's arguments and remarks are addressed. The Examiner has determined that the previous Office Action is still proper based on the above responses. Therefore, the rejections are sustained and maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 35 – 36, 40 – 41, 46 – 48, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher et al. (U.S. Pat. No. 6,614,103 B1), hereinafter as Durocher, and further in view of Okazaki et al. (U.S. Pat. App. Pub. No. 2003/0062530 A1), hereinafter as Okazaki.

Regarding claim 35, figs. 12 – 13 of Durocher teaches a semiconductor light emitting device comprising:

a base substrate (refs. 31 and/or 41);

a pair of power supply terminal thin-film layers (one of each ref. 47; col. 9, lines 29 – 31), each being provided on different areas of a first main surface of the base substrate (as seen in figs. 12 – 13, each of ref. 47 are in different areas on the bottom of ref. 41 or portions of ref. 37 in refs. 53,55 areas and bottom of ref. 31), and the pair of power supply terminal thin-film layers (e.g., one of LED pair electrode terminals) being electrically connected to each other via through-holes (refs. 37 and 49) provided in the base substrate (as seen in figs. 12 – 13), wherein

a second main surface of the base substrate (as seen in figs. 12 - 13, top of refs. 31 and/or 41) has provided thereon a semiconductor multilayer epitaxial structure (ref. no. 59; col. 7, lines 30 – 40; see teaching of Okazaki below for multilayer epitaxial structure), and

a phosphor film (ref. 65) covers the semiconductor multilayer epitaxial structure.

Durocher may not explicitly teach the following limitations whereas figs. 1 and 3D of Okazaki teaches it is known in the art to provide:

a semiconductor multilayer epitaxial structure (§0049) including a first conductive layer (ref. no. 2), a light emitting layer (ref. no. 3), and a second conductive layer (ref. no. 4) formed in the stated order (as combined with the teaching of figs. 12 – 13 of Durocher and fig. 3A of Okazaki),

a first electrode thin-film layer (ref. 5a) is in contact with the first conductive layer,
a second electrode thin-film layer (ref. 13) is in contact with the second conductive layer, and

a first thin-film layer (ref. 5b) and a second thin-film layer (ref. 6) electrically connect the first electrode thin-film layer and the second electrode thin-film layer respectively (as seen in figs. 1 and 3A) via the through-holes (as combined with figs. 12 – 13 of Durocher).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher with the light emitting device of Okazaki, in order to provide improved external quantum efficiency light emitting devices (§0040). It is proper to combine Durocher and Okazaki because they both teach analogous art relating to light emitting devices.

Regarding claim 36, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher teaches wherein the multilayer epitaxial structure is formed on the base substrate leaving a space along each edge of a main surface of

the base substrate which faces the multilayer epitaxial structure (as seen in fig. 12, next to each LED, ref. no. 59, are spaces); and

the first through hole and the second through hole are provided in a peripheral portion of the base substrate, the peripheral portion corresponding to the space (as seen in fig. 12, at the left and the right peripheral sides of the LEDs).

Regarding claim 40, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher and Okazaki teaches wherein the multilayer epitaxial structure having a structural characteristic of epitaxial growth (§0049 of Okazaki) on a single-crystal substrate (ref. no. 1 and §0039 of Okazaki) different from the base substrate (col. 5, lines 17 – 31 of Durocher), and is mounted on the base substrate (as combined and would have been seen just as figs. 12 – 13 of Durocher with fig. 1 of Okazaki).

Regarding claim 41, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 40, Durocher and Okazaki teaches wherein the multilayer epitaxial structure is mounted to the base substrate in such a manner that a last epitaxially-grown layer (ref. no. 2 of Okazaki; see note 1 below) having grown on a single-crystal substrate (ref. no. 1 and §0039 of Okazaki) different from the base substrate is positioned closer to the base substrate than a first epitaxially-grown layer (ref. no. 4 of Okazaki; see note 1 below) is.

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Because the product by process does not change the end product, Applicant's claimed invention does not distinguish over prior art. See MPEP § 2113.

In the instant case, the first and last epitaxially-grown layers as recited are oppositely grown by what is taught by ¶0049 of Okazaki. Okazaki teaches that ref. no. 2 layer was one of the first to grow and ref. no. 4 is grown thereafter. However, chronological ordering of when the layers are epitaxially-grown would not have changed the end result of the product, as Okazaki's end product rendered the claimed invention obvious when mounted on Durocher's substrate carrier in two positions as illustrated in figs. 12 – 13.

Regarding claim 46, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher teaches wherein the first and the second through holes are positioned in a periphery of the base substrate (as seen in fig. 12, next to each LED, ref. no. 59, are spaces at the left and the right peripheral sides of the LEDs), and the multilayer epitaxial structure is not positioned on or over the first and second through holes (as seen in fig. 12).

Regarding claim 48, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher and Okazaki teaches wherein the multilayer epitaxial structure is mounted on the base substrate in such a manner that a last epitaxially-grown layer (ref. no. 2 of Okazaki; see note 1 below) having a structure characteristic (§0049 of Okazaki) of being grown on a single-crystal substrate (ref. no. 1 and §0039 of Okazaki) different from the base substrate (col. 5, lines 17 – 31 of Durocher) is positioned closer to the base substrate (as combined and would have been seen just as figs. 12 – 13 of Durocher with fig. 1 of Okazaki) than a portion of a first epitaxially-grown layer (ref. no. 4 of Okazaki; see note 1 below).

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Because the product by process does not change the end product, Applicant's claimed invention does not distinguish over prior art. See MPEP § 2113.

In the instant case, the first and last epitaxially-grown layers as recited are oppositely grown by what is taught by §0049 of Okazaki. Okazaki teaches that ref. no. 2 layer was one of the first to grow and ref. no. 4 is grown thereafter. However, chronological ordering of when the layers are epitaxially-grown would not have changed

the end result of the product, as Okazaki's end product rendered the claimed invention obvious.

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher and Okazaki as applied to claim 35 above, and further in view of Baik et al. (U.S. Pat. App. Pub. No. 2004/0108511 A1), hereinafter as Baik.

Regarding claim 37, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, but Durocher and Okazaki may not explicitly teach the following limitations whereas Baik teaches that it is known in the art to provide further comprising:

a metal reflective film (ref. nos. 35, 37 and/or 39) that is sandwiched between the multilayer epitaxial structure (ref. nos. 24, 26 and 28) and the base substrate (Durocher's ref. no. 41 as seen in figs. 12 – 13).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher and Okazaki with the reflective film of Baik, in order to provide excellent reflective characteristics (¶10018). It is proper to combine Durocher, Okazaki and Baik because they both teach analogous art relating to light emitting devices.

Claims 35 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing Chen et al. (U.S. Pat. App. Pub. No. 2004/0188696 A1), hereinafter as Hsing Chen.

Regarding claim 35, figs. 9 – 10 of Hsing Chen discloses a semiconductor light emitting device comprising:

a base substrate (ref. 710); and

a pair of power supply terminal thin-film layers (ref. 714), each being provided on different areas of a first main surface of the base substrate (e.g., left and right sides as seen in fig. 9), and the pair of power supply terminal thin-film layers being electrically connected to each other via through-holes (where ref. 714 points at in ref. 710) provided in the base substrate (as seen in fig. 9), wherein

a second main surface of the base substrate has provided thereon a semiconductor multilayer epitaxial structure including a first conductive layer (ref. 740; ¶32 and 52), a light emitting layer (ref. 734; ¶32 and 52), and a second conductive layer (ref. 734; ¶32 and 52) formed in the stated order,

a first electrode thin-film layer (ref. 744) is in contact with the first conductive layer,

a second electrode thin-film layer (ref. 740) is in contact with the second conductive layer;

a phosphor film (ref. 760; see ¶50, ref. 560, obvious for light conversion) covers the semiconductor multilayer epitaxial structure (as seen in fig. 9), and

a first thin-film layer (one of ref. 750 on ref. 716) and a second thin-film layer (one of ref. 750 on ref. 716) electrically connect the first electrode thin-film layer and the second electrode thin-film layer respectively via the through-holes (as seen in fig. 9).

Regarding claim 52, Hsing Chen discloses the semiconductor light emitting device of Claim 35, wherein the phosphor layer covers an entirety of the base substrate, including surrounding edge portions of the base substrate (as seen in fig. 9, ¶52; also see fig. 10, ¶54), and a peripheral lateral surface of the base substrate and a peripheral lateral surface of the phosphor layer are a continuous surface (as seen in fig. 9, ¶52; also see fig. 10, ¶54).

Allowable Subject Matter

Claim 49 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The examiner notes that if applicant chooses to include claims 48 – 49 into claims 35 for allowance, claim 41 should be reviewed because claim 48 includes substantially similar claim language as claim 41.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious, *inter alia*, the multilayer epitaxial structure mounting on

the base substrate with its structure characteristic, wherein the base substrate is a SiC substrate.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan T. Ho whose telephone number is 571-272-8711. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoang-Quan T Ho/
Examiner, Art Unit 2818
February 27, 2009

/Andy Huynh/
Primary Examiner, Art Unit 2818